

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Cheng-Lien Chiang
Assignee: Bridge Semiconductor Corporation
Title: METHOD OF MAKING A SEMICONDUCTOR PACKAGE
DEVICE
Serial No.: Unknown Filed: Herewith
Examiner: Unknown Group Art Unit: Unknown
Atty. Docket No.: BDG005-1

31000 U.S. PTO
10/059686
01/29/02

FD
HDS
905-L2
253

ASSISTANT COMMISSIONER FOR PATENTS
Washington, D.C. 20231

INFORMATION DISCLOSURE STATEMENT


Pursuant to Applicant's duty of disclosure under 37 C.F.R. § 1.56 and §§ 1.97-1.98, Applicant hereby submits the enclosed Form PTO-1449.

Copies of documents cited on the enclosed Form PTO-1449 are not enclosed because they were previously cited by or submitted to the U.S. Patent Office in prior U.S. Application Serial No. 10/042,812 filed January 9, 2002. The above-identified application is a continuation of the prior application.

The filing of this Information Disclosure Statement shall not be construed as a representation that a search has been made, an admission that any of these documents, alone or in any combination, is considered to be material to patentability, an admission that any of these documents is prior art as to the above-identified application, or an admission against interest in any manner.

This Information Disclosure Statement is filed before the mailing date of a first Office Action. Accordingly, no fee is due.

Respectfully submitted,

A handwritten signature in black ink, appearing to read "D Sigmond". The signature is written in a cursive, flowing style.

David M. Sigmond
Attorney for Applicant
Reg. No. 34,013
(303) 554-8371
(303) 554-8667 (fax)

Form PTO-1449	Atty Docket No.	Serial No.
U.S. Department of Commerce, Patent and Trademark Office	BDG005-1	
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	Applicant Cheng-Lien Chiang	
	Filing Date	Group Art Unit

10/05/98
10/29/02

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	5,081,520	01/1992	Yoshii et al.	357	80	
	AB	5,241,133	08/1993	Mullen, III et al.	174	52.4	
	AC	5,394,303	02/28/95	Yamaji	361	749	
	AD	5,665,652	09/1997	Shimizu	438	127	
	AE	5,674,785	10/1997	Akram et al.	437	217	
	AF	5,744,827	04/28/98	Jeong et al.	257	686	
	AG	5,744,859	04/1998	Ouchida	257	668	
	AH	5,804,771	09/1998	McMahon et al.	174	255	
	AI	5,811,879	09/1998	Akram	257	723	
	AJ	5,949,655	09/1999	Glenn	361	783	
	AK	6,013,877	01/2000	Degani et al.	174	264	
	AL	6,143,588	11/2000	Glenn	438	116	
	AM	6,159,770	12/2000	Tetaka et al.	438	112	
	AN	6,274,927	08/2001	Glenn	257	680	

Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)

AO	Crowley, "Socket Developments for CSP and FBGA Packages," Chip Scale Review, May 1998, pp. 37-40.
AP	Forster, "Socket Challenges for Chip-Scale Packages," Chip Scale Review, May 1998, pp. 43-47.
AQ	Amagai, "Chip-Scale Packages for Center-Pad Memory Devices," Chip Scale Review, May 1998, pp. 68-77.
AR	Vandavelde et al., "The PSGA, a Lead-Free CSP for High Performance & High Reliable Packaging," Proceedings of the 2001 International Symposium on Microelectronics, October 9, 2001, pp. 260-265.

Examiner

Date Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your next communication to Applicant.

Form PTO-1449		Atty Docket No.	Serial No.
U.S. Department of Commerce, Patent and Trademark Office		BDG005-1	
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)		Applicant Cheng-Lien Chiang	
		Filing Date	Group Art Unit
*Examiner Initial	Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)		
	AA	U.S. Application Serial No. 09/865,367, filed May 24, 2001, entitled "Semiconductor Chip Assembly With Simultaneously Electroplated Contact Terminal and Connection Joint"	
	AB	U.S. Application Serial No. 09/864,555, filed May 24, 2001, entitled "Semiconductor Chip Assembly with Simultaneously Electrolessly Plated Contact Terminal and Connection Joint"	
	AC	U.S. Application Serial No. 09/864,773, filed May 24, 2001, entitled "Semiconductor Chip Assembly With Ball Bond Connection Joint"	
	AD	U.S. Application Serial No. 09/878,649 filed June 11, 2001, entitled "Method of Making a Semiconductor Chip Assembly with a Conductive Trace Subtractively Formed Before and After Chip Attachment"	
	AE	U.S. Application Serial No. 09/878,626 filed June 11, 2001, entitled "Method of Connecting a Conductive Trace to a Semiconductor Chip"	
	AF	U.S. Application Serial No. 09/917,339 filed July 27, 2001, entitled "Method of Connecting a Bumped Compliant Conductive Trace to a Semiconductor Chip"	
	AG	U.S. Application Serial No. 09/927,216 filed August 10, 2001, entitled "Semiconductor Chip Assembly with Hardened Connection Joint"	
	AH	U.S. Application Serial No. 09/939,140 filed August 24, 2001, entitled "Semiconductor Chip Assembly with Interlocked Conductive Trace"	
	AI	U.S. Application Serial No. 09/962,754 filed September 24, 2001, entitled "Method of Connecting a Conductive Trace and an Insulative Base to a Semiconductor Chip"	
	AJ	U.S. Application Serial No. 09/972,796 filed October 6, 2001, entitled "Method of Connecting a Bumped Compliant Conductive Trace and an Insulative Base to a Semiconductor Chip"	
	AK	U.S. Application Serial No. 09/997,973 filed November 29, 2001, entitled "Method of Connecting a Bumped Conductive Trace to a Semiconductor Chip"	
Examiner		Date Considered	
<p>*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your next communication to Applicant.</p>			